

CLAIMS

What is claimed is:

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SUB A1 7 1. A circuit for controlling a rise-time of a signal, comprising:  
a voltage multiplication circuit which converts an input voltage to  
an output voltage greater than said input voltage;  
a switched capacitor circuit coupled to said voltage multiplication  
circuit which controls said output voltage from said voltage  
10 multiplication circuit, wherein a ratio between a first capacitor of said  
switched capacitor circuit and a second capacitor of said switched capacitor  
circuit determines said rise-time of said signal.
- 15 SUB C2 2. The circuit of Claim 1, wherein said voltage multiplication  
circuit comprises a charge pump.
3. The circuit of Claim 1, wherein said signal is used to program  
and erase Flash EPROM cells.
- 20 4. The circuit of Claim 1 further comprising a constant ramp  
generator. A
5. The circuit of Claim 1, wherein said signal comprises a stair-  
case/ramp signal. SUB C2
6. The circuit of Claim 1, wherein said voltage multiplication  
circuit generates a VPP output voltage given a VCC input voltage.

7. The circuit of Claim 1 further comprising a level shifter to shut off said signal.

5 8. The circuit of Claim 1 further comprising two non-overlapping clock signals.

9. The circuit of Claim 1 further comprising a ring oscillator coupled to said switched capacitor circuit.

10 10. The circuit of Claim 1 further comprising a capacitor divider network coupled to said switched capacitor circuit.

11. The circuit of Claim 1, wherein said switched capacitor circuit switches between ground and a divider node which has a constant reference voltage according to a feedback system.

12. The circuit of Claim 11, wherein said feedback system comprises a CMOS comparator.

13. The circuit of Claim 1 further comprising a divide by N counter.

SUB A2  
25 14. A switched capacitor controller for controlling a rise time of an on-chip generated voltage source, comprising:  
a charge pump;  
a ramp generator coupled to said charge pump

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- a switched capacitor coupled to said ramp generator;  
a regulator circuit coupled to said switched capacitor which causes a capacitor to switch between ground and a node, wherein a stair-step ramp signal is generated and said rise time is controlled according to said  
5 switched capacitor.

15. The switched capacitor controller of Claim 14, wherein said rise time is controlled according to a ratio of two capacitors.

16. The switched capacitor controller of Claim 14, wherein said on-chip generated voltage source is used to program a Flash memory.

17. The switched capacitor controller of Claim 14 further comprising an oscillator coupled to said charge pump which generates an oscillating signal input to said charge pump.  
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18. The switched capacitor controller of Claim 17 further comprising:

- a divider coupled to said oscillator;  
20 a non-overlapping two phase clock generator coupled to said divider.

19. The switched capacitor controller of Claim 14, wherein said ramp generator further comprises a capacitor divider network.  
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20. In a flash memory, a method for controlling a rise time of an on-chip generated voltage source used to program said flash memory, comprising:

- generating a programming voltage from a power supply, wherein  
5 said programming voltage is greater than voltage from said power supply;  
activating a program signal to program a cell of said flash memory;  
generating a stair-case ramp based on said programming voltage in  
response to said program signal, wherein steps of said stair-case ramp have  
a period corresponding to a clock signal and voltage increases  
10 corresponding to a reference voltage times a ratio of two capacitor values.

21. The method of Claim 20 further comprising the step of  
switching a capacitor between ground and a node voltage to generate said  
stair-case ramp.